**New York Institute of Technology**

**School of Engineering and Computing Sciences**

NYIT Academy Summer Camp

VHDL Assignment 1

Introduction: Combinatorial and Sequential Logic Using Model-Sim

1. Enter this code into the Model-Sim Text Editor window.

--Library contains standard VHDL logic

Library ieee;

Use ieee.std\_logic\_1164.ALL;

--Entity defines inputs and output

Entity TEST is

Port (

A, B : in std\_logic;

Y : out std\_logic);

End TEST;

--Architecture describes circuit functionality

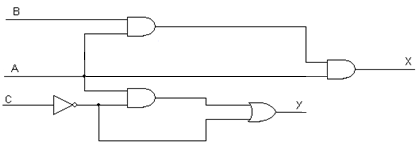
Architecture LOGIC\_FUNCTION of TEST is

Begin

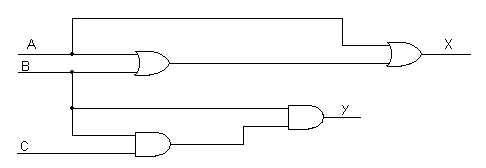
Y <= (A and B);

End LOGIC\_FUNCTION;

1. Implement the above code by using ModelSim.
2. Write aVHDL code to implement the following logic expression using ModelSim:
   1. M = (AB)+(CD)
   2. P = (AC+BC)(A+C)



d.



1. **Be sure to prepare a truth table.**